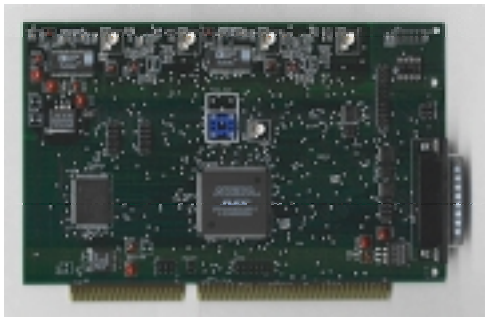
Addendum to PulseBlaster Owner's Manual

Revised Board Layout – PulseBlaster™ and PulseBlasterDDS™



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1. Header/Jumper Information

J4: Selecting ISA Bus Address **(Pins 1-2, 3-4, and 5-6).**

The Base Addresses that can be specified for the ISA PulseBlaster™ and PulseBlasterDDS™ boards can range from 0x260 to 0x360. The default, factory pre-set value is 0x340. This value can be changed, via jumpers on Header J4, according to the Table 1.

Base Address (in Hex)	Jumper Settings – Header J4 Pins 5-6	Pins 3-4	Pins 1-2
300	|	|	|
320	|	|	:
340	|	:	|
260	|	:	:
280	:	|	|
270	:	|	:
290	:	:	|
360	:	:	:

Table 1. Board's ISA-Bus Base Address Selection
(Legend: | jumper across pins, : no jumper)

(Default Value = 0x340, jumpers 1-2, 5-6).

JPower1 and JPower2: Selecting output voltage levels

The digital (TTL) output signals are driven by latches/drivers capable of running off a 5.0-V or 3.3-V supply. The supply voltage for the drivers is selectable. Table 2, below, lists the configurations for 5.0-V and 3.3-V output driver operation.

5 V Operation
Jumper JPower1-1 across to JPower1-2
Jumper JPower2-1 across to JPower2-2
3.3 V Operation
Jumper JPower1-3 across to JPower1-4
Jumper JPower2-3 across to JPower2-4

Table 2. Output voltage selection

The JPower1 header selects the operating voltage for the output bits 0-15, and JPower2 independently selects the operating voltage for the output bits 16-23.

JTrigger: External trigger/reset lines.

The Jtrigger header contains two active pins (pins 1 and 3) and two ground pins (pins 2 and 4). The **HW_Trigger** line (pin 1) is pulled high (via a 10-kohm resistor) by default. When a falling edge is detected (e.g., when shorting pins 1-2, pin 2 = ground), it initiates code execution. This trigger will also restart execution of a program from the beginning of the code if it is detected after the design has reached an idle state. The idle state could have been created either by reaching the WAIT Op Code of a program, or by the detection of the HW_Reset signal.

The **HW_Reset** line (pin 3) is pulled high by a 10-kohm resistor. It can be used to halt the execution of a program by pulling it low (e.g., by shorting pins 3-4, pin 4 = ground). When the signal is pulled low during the execution of a program, the controller resets itself back to the beginning of the program. Program execution can be resumed by either a software start command or by a hardware trigger.

J9 and DB25 (J10) : Output Bits, J12: Status

The following table lists the output bits (TTL levels) for the PulseBlaster™ and PulseBlasterDDS™ Pulse/Pattern/RF Generator Boards:

Signal	Location
Bit 0	J10-13
Bit 1	J10-25
Bit 2	J10-24
Bit 3	J10-11
Bit 4	J10-10
Bit 5	J10-22
Bit 6	J10-21
Bit 7	J10-8
Bit 8	J10-7
Bit 9	J10-19
Bit 10	J10-18
Bit 11	J10-5
Bit 12	J10-4
Bit 13	J10-16
Bit 14	J10-15
Bit 15	J10-1
Bit 16	J9-15
Bit 17	J9-13
Bit 18	J9-11
Bit 19	J9-9
Bit 20	J9-7
Bit 21	J9-5
Bit 22	J9-3
Bit 23	J9-1
Output Clock	J10-1
Running	J12-1
Stopped	J12-5
System Reset	J12-3

Table 3. Output bits and signal assignments of the PulseBlaster™ and PulseBlaster™ boards.

Bits 15-0 are grouped on the external DB-25 connector (also marked as J10) provided for accessing the signals. The rest of the bits, Bits 23-16, are accessible on an internal IDC header J9. (NOTE: depending on the design, some of the output bits may not be available). The table also lists several additional output signals that are available to the outside world via header J12. All remaining pins on the DB-25 and all even pins of J9 connector are connected to the ground.

2. Header/Jumper Location

The location of the relevant headers and connectors on the PulseBlaster™ and PulseBlasterDDS™ boards is presented in Figure 1.

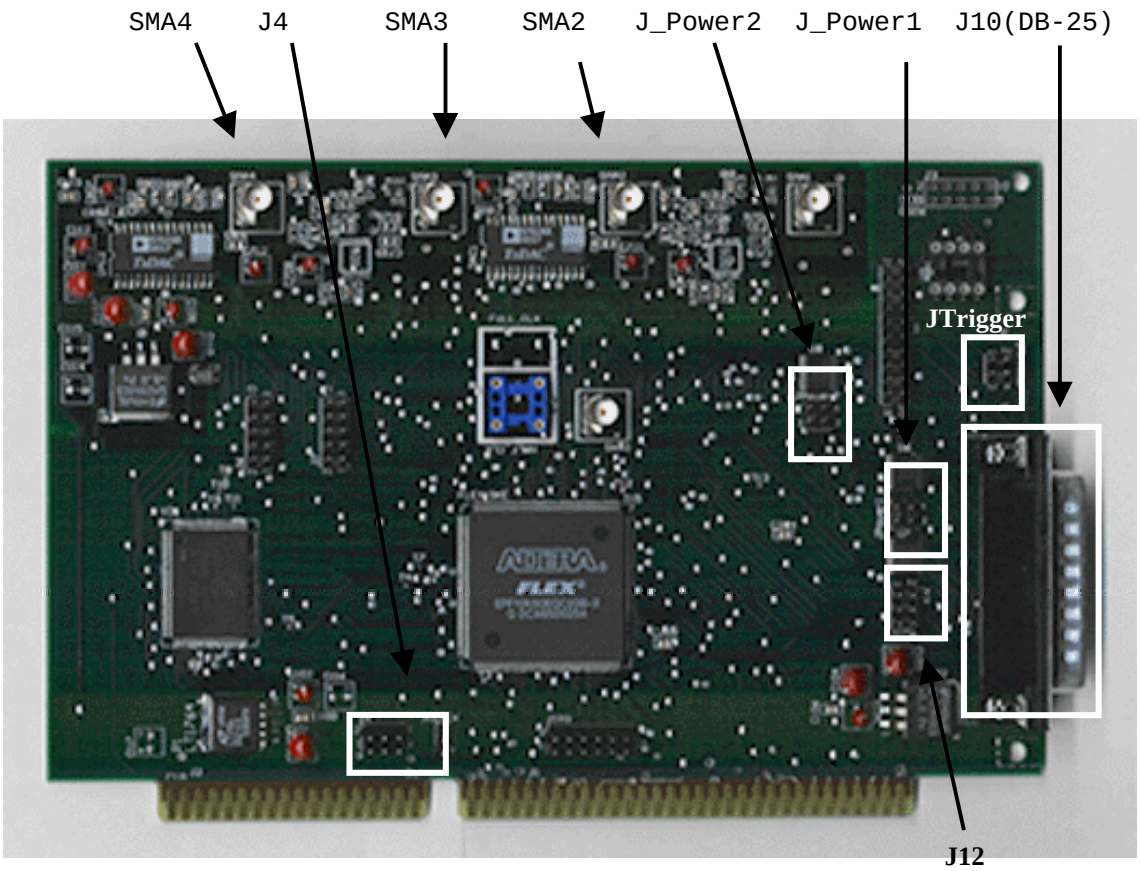

Figure 1. PulseBlaster™ and PulseBlasterDDS™ boards – header/connector locations.

3. SMA1-SMA5 – Optional RF/AWG/Clock Connectors

SMA1-SMA4 are optional RF connectors that can be used to output RF frequencies or arbitrary waveforms generated by the board equipped with Direct Digital Synthesis and Arbitrary Waveform Generator cores (PulseBlasterDDS™). Output impedance is 50 ohms; output amplitude is approx. 0 dB_{mW}; max RF frequency is ½ master (reference) clock frequency, down to DC; max update rate of AWG samples equals the max. master (reference) clock frequency of the board.

SMA5 is a connector that can be used to input an external master clock signal. When equipped, the connector is terminated with a 50-ohm resistor and TTL signal levels are expected on the connector's input pin (any negative voltage present on SMA5 will damage the board's processor chip).