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# PulseBlasterDDS-IV-1000

## Owner's Manual

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SpinCore Technologies, Inc.

<http://www.spincore.com>

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# ***PulseBlasterDDS-IV-1000***

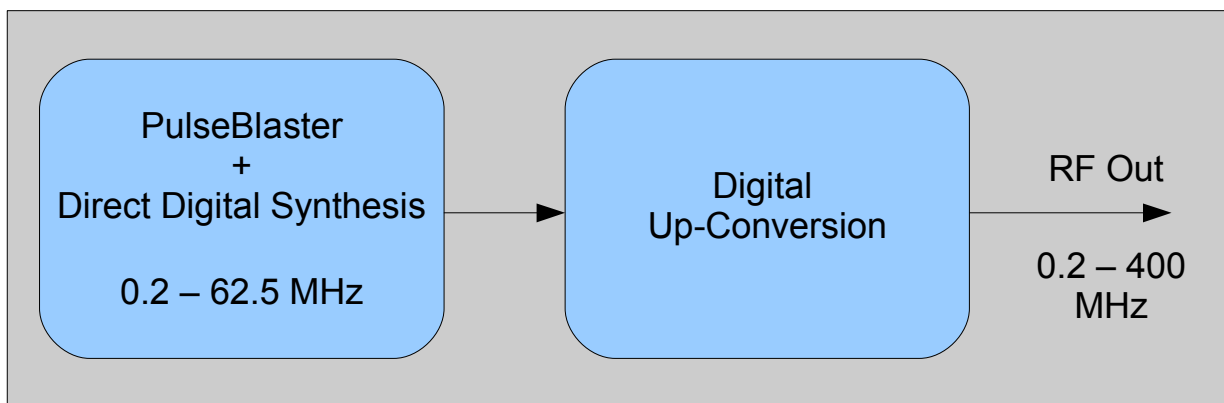
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## I. Introduction

### Product Overview

The PulseBlasterDDS-IV-1000 is a programmable Intelligent Pattern and Waveform Generation system from SpinCore Technologies, Inc. that couples SpinCore's unique Intelligent Pattern Generation processor core, the PulseBlaster, with two Direct Digital Synthesis (DDS) units for use in system control and pulse generation. By interfacing the system with a high performance Analog Devices AD9148 Quad DAC (Digital to Analog Converter) operating at a sampling frequency of 1000 MS/s, a range of RF (Radio Frequency) signals can be produced from 200 kHz to 400 MHz. Additionally, 16 independent, programmable digital (TTL logic) pulses can be generated with the PulseBlaster core to produce sophisticated pulse sequences.

The DDS-IV is a complete high frequency excitation system for high field NMR, MRI, NQR, spintronics, quantum computing, and related resonance and testing technologies up to 400 MHz.



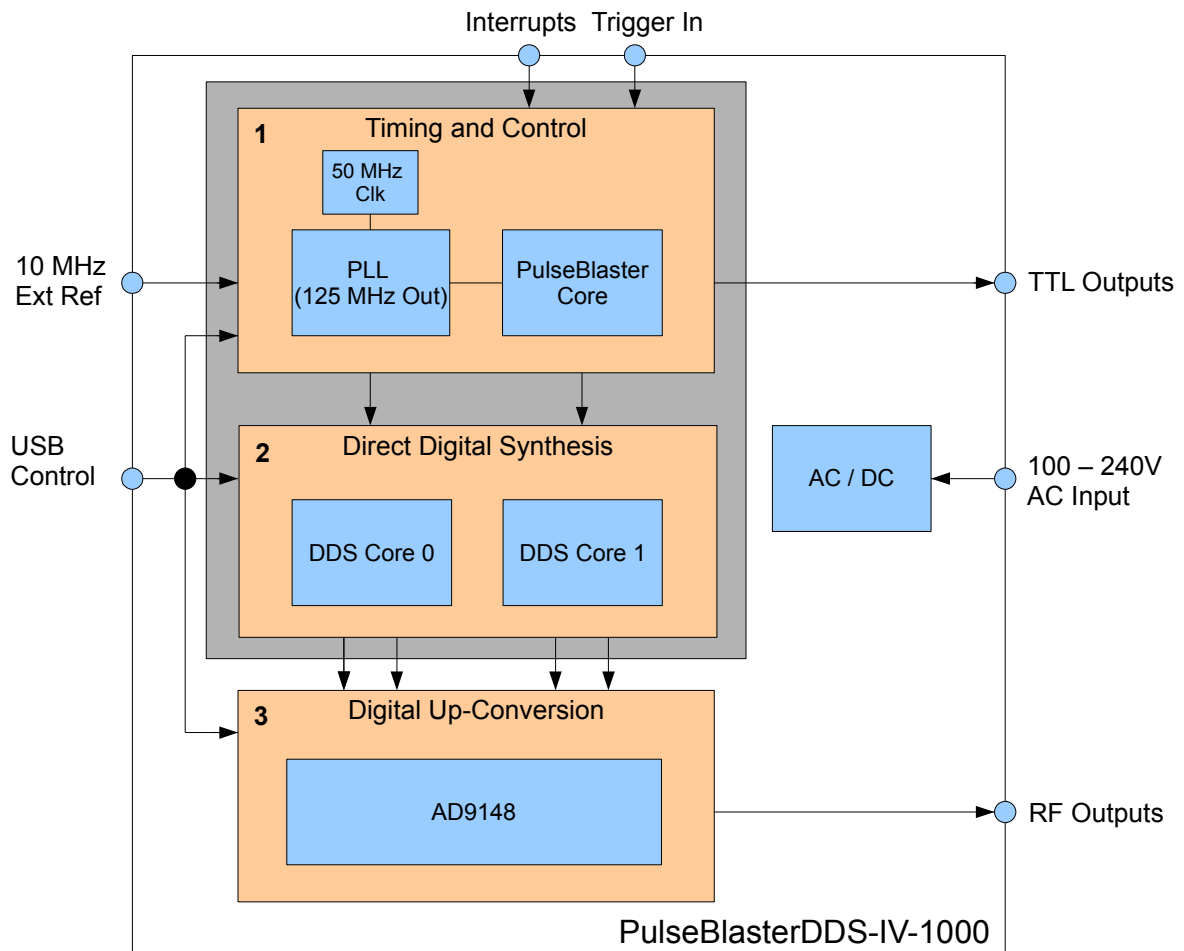
**Figure 1:** This simple block diagram illustrates the basic concept of the PulseBlasterDDS-IV-1000 system. The DDS cores produce patterns in the base-band range of 0.2 to 62.5 MHz. These signals are then digitally up-converted and placed in the desired output band up to 400 MHz. See the next section, Product Architecture, for a more detailed description of the implementation of this concept. See the section Configuring the Output Frequencies for more information on the digital up-conversion features of the system.

#### **Key Features**

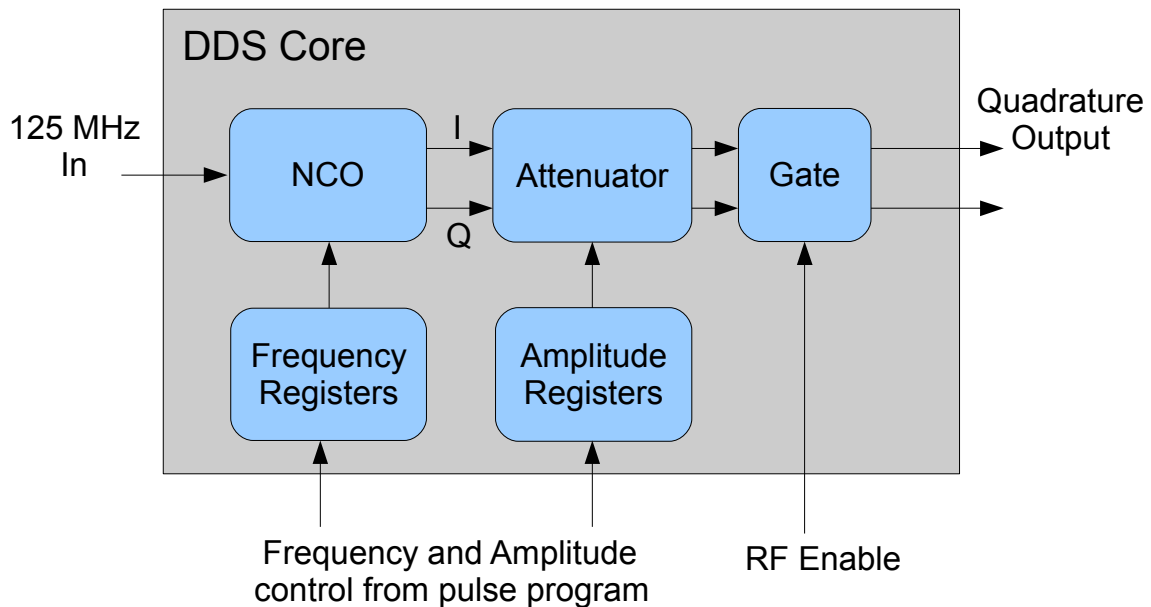
- Two independent, programmable DDS cores that can output RF signals up to 400 MHz.
- Each independent DDS core is equipped with two quadrature outputs for a total of four RF outputs.
- 16 digital, TTL outputs with pulse resolutions of 8 ns.
- Advanced pulse program flow features including loops, subroutines, and interrupts.
- 256 programmable interrupts (interrupts are immediate and always active).

## Product Architecture

Figure 2, shown below, presents the general architecture of the PulseBlasterDDS-IV-1000 system. The three major building blocks of the DDS-IV are the PulseBlaster Programming and Timing Processor Core (1), the two independent DDS Cores (2), and the AD9148 DAC (3). The DDS and PulseBlaster cores have been implemented in programmable logic on an Altera Stratix III FPGA (Field-Programmable Gate Array) chip.



**Figure 2:** This is a block diagram of the basic architecture of the PulseBlasterDDS-IV-1000. The PulseBlaster core provides the intelligence that directs the DDS units which in turn provide the digital data that the AD9148 translates into RF signals. The PulseBlaster core also outputs 16 independent digital pulses, each with a timing resolution of 8 nanoseconds.



**Figure 3:** The basic block diagram of the Direct Digital Synthesis (DDS) core. The PulseBlaster core provides the control signals that configure the DDS cores to output signals at the desired frequency and amplitude.

Figure 3, shown above, presents the basic architecture of the Direct Digital Synthesis (DDS) core. There are two such cores in the DDS-IV system that provide two independent output streams. The NCO (Numerically Controlled Oscillator) provides a quadrature data, or In-Phase (I) and a Quadrature (Q) parts, for each stream.

The NCO operates with a 125 MHz clock frequency and is configured by user programmable 256 frequency registers. There are also 128 programmable amplitude registers that can be used to attenuate RF outputs or modulate output amplitude.

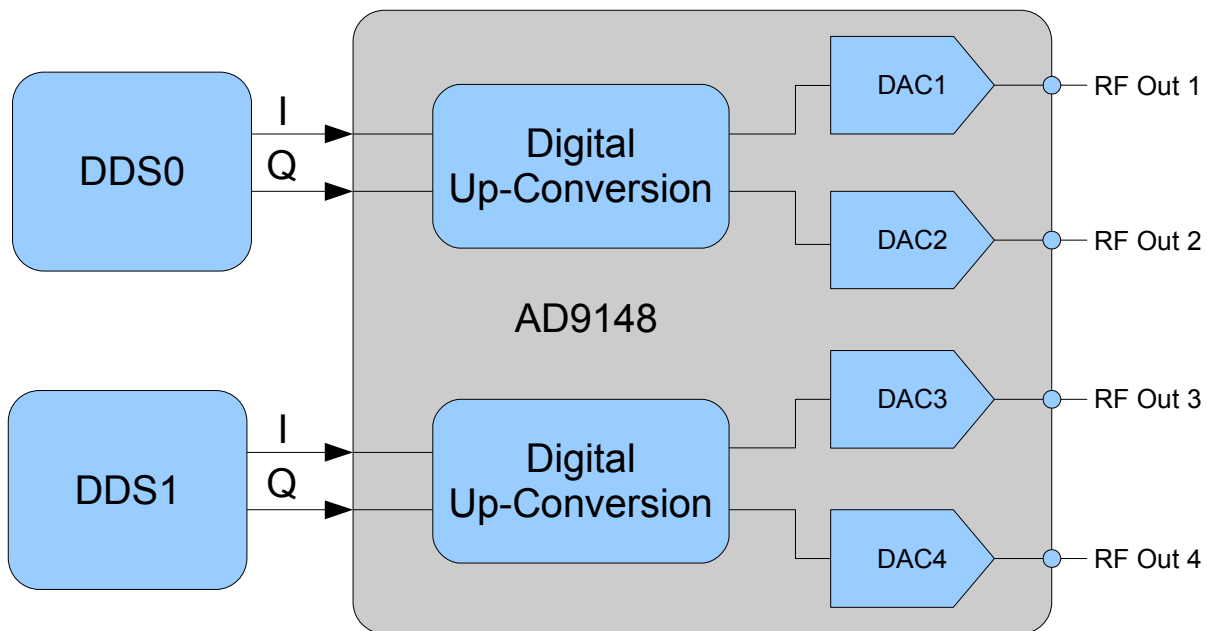
The PulseBlaster Core controls the timing of gating the RF pulses and provides the necessary control signals for the frequency and amplitude registers. In addition, the PulseBlaster core generates 16 independent digital outputs for direct use.

# PulseBlasterDDS-IV-1000

A more detailed diagram of the interface between the PulseBlasterDDS cores and the AD9148 DAC is presented below in Figure 4. The AD9148 contains digital half-band interpolation filters which can be configured to shift the base-band frequencies produced by the DDS cores up to higher frequencies. When all of the half-band interpolation filters are used together, the maximum interpolation ratio of 8x is achieved and the AD9148 will interpolate 8 samples of data for every 1 sample it receives from the DDS cores.

In order to ensure that the half-band interpolation filters can be adjusted to produce all frequencies up to 400 MHz the data generated by the DDS cores must be a quadrature stream. The quadrature stream consists of two parts: an In-Phase (I) and a Quadrature (Q) data pattern that are offset by 90 degrees but represent a single signal.

Each DDS core outputs a quadrature stream into one of the two complex digital data paths within the AD9148. The two complex data paths within the AD9148 feed the four DAC outputs. Consequently, only two of the DAC outputs (Output 1 and Output 3) generate independent waveforms. Output 2 will produce the same wave as Output 1 with a phase offset of 90 degrees. The same relationship applies to Outputs 3 and 4.



**Figure 4:** This diagram gives a cursory overview of how the DDS cores interact with the AD9148 DAC. The DDS cores output quadrature data streams (I and Q pairs) to the input ports of the AD9148. The digital up-conversion functionality consist of half-band interpolation filters that are used to shift base-band frequencies from the DDS cores to higher intermediate frequencies (up to the Nyquist rate). Any desired output higher than 62.5 MHz requires the use of these digital up-conversion features.

## Product Specifications

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	<i>Parameter</i>	<i>Min</i>	<i>Typical</i>	<i>Max</i>	<i>Units</i>
Analog Output	D/A sampling rate		1000		MHz
	D/A sampling precision			14	bits
	Output voltage range (peak-peak, terminated with a 50 Ohm load)			1.05	V
	Frequency resolution		0.12		Hz
	TTL to RF Latency		508		ns
Digital Output	Number of digital outputs		16		
	Logical 1 output voltage		3.3 <sup>1</sup>		V
	Logical 0 output voltage		0		V
	Output drive current			66	mA
	Rise/Fall time			< 1	ns
Digital Input	Number of Interrupts		256		
	HW Interrupt Activation Level	2.5		3.3	V
	HW Trigger/Reset Activation Level			0.8	V
	10 MHz Clock Input Reference Voltage, Square Wave			3.3	V
Pulse Program	Number of instruction words		8K		words
	Pulse timing resolution		8		ns
	Instruction time length	40 ns		693 days	

**Table 1:** Technical specifications for the DDS-IV-1000.

<sup>1</sup> This is the unterminated voltage. The required minimum logical high TTL level of 2.5 V is attained when the load impedance is 150 Ω.

<sup>2</sup> The phase register feature is currently unsupported. If you require this feature, please contact SpinCore Technologies.

## **II. Using the PulseBlasterDDS-IV-1000 API**

In order to configure the PulseBlasterDDS-IV-1000, there are two software interfaces that must be used: the AD9148 DAC configuration program, and the PulseBlasterDDS-IV-1000 API. These two interfaces will work together to allow frequencies of up to 400 MHz to be produced.

### **Controlling the PulseBlasterDDS-IV-1000**

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This section describes the function and use of each feature of the PulseBlasterDDS-IV-1000 API.

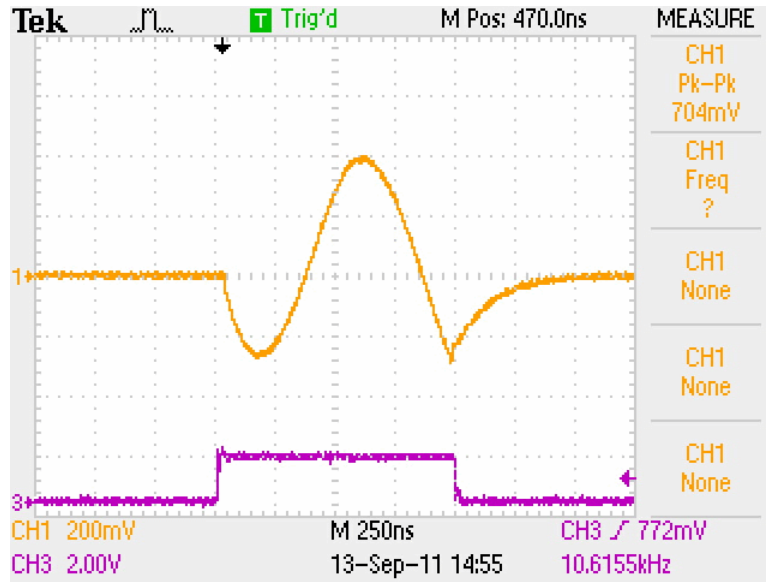
The PulseBlasterDDS-IV-1000 is a highly versatile excitation system and there are several options for programming it. The following steps outline the basic approach to programming and running a program on the DDS-IV:

1. Load frequency and amplitude registers with the desired values.
2. Set up the DAC configuration software to output the desired frequency range.
3. Specify a pulse program which will control the timing of the experiment.
4. Trigger the pulse program. The experiment will then proceed autonomously.

The PulseBlasterDDS-IV API is a control library which allows programs to be written to communicate with your SpinCore board. The most straightforward way to interface with this library is with a C/C++ program, and the API definitions are described in this context. However, virtually all programming languages and software environments (including software such as LabView and Matlab) provide mechanisms for accessing the functionality of standard libraries such as the PulseBlasterDDS-IV API.

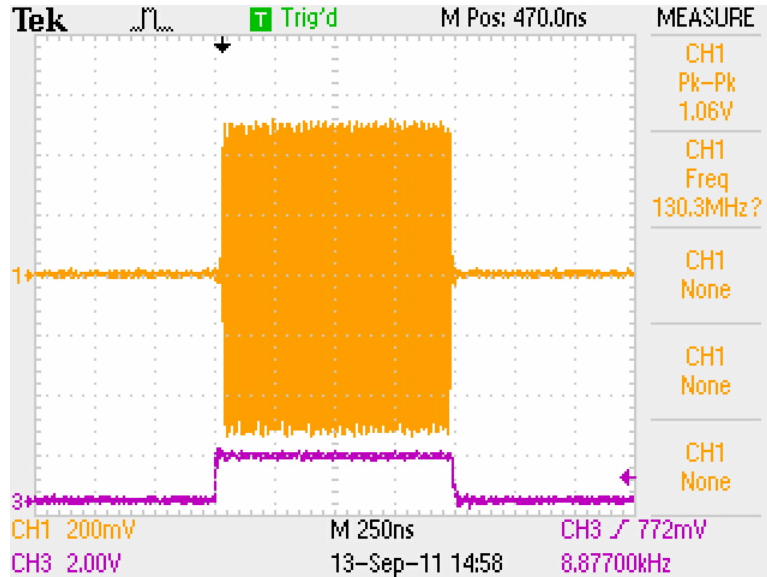
## Sample Output

In this section you will find oscilloscope screen captures of the PulseBlasterDDS-IV-1000 system running through its example and other test programs. All screen shots were captured with a Tektronix TDS 2024B. This scope greatly attenuates high frequency signals over 200 MHz.

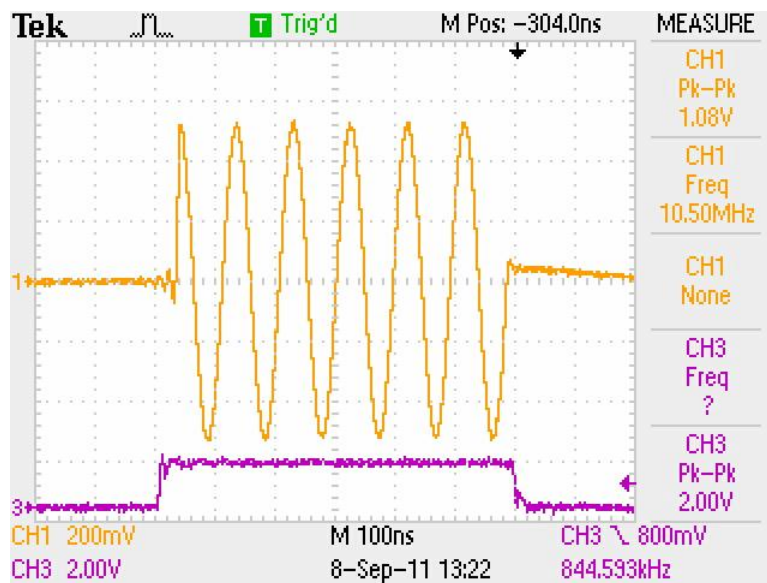


**Figure 5:** A 1000 ns 1 MHz RF pulse is shown in the base band with no digital up-conversion features enabled. The 500 ns stabilization time after the RF gate is disabled is associated with the AD9148 DAC at lower frequencies.

# PulseBlasterDDS-IV-1000

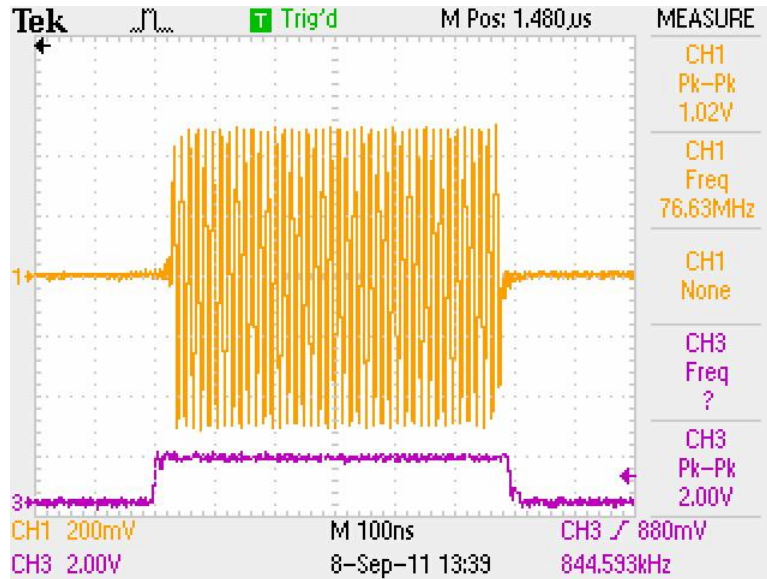


**Figure 6:** The digital up-conversion option "Fs/8" has been applied to the signal from Figure 5. The signal is shifted up by one-eighth of the DAC sampling rate, or 125 MHz.

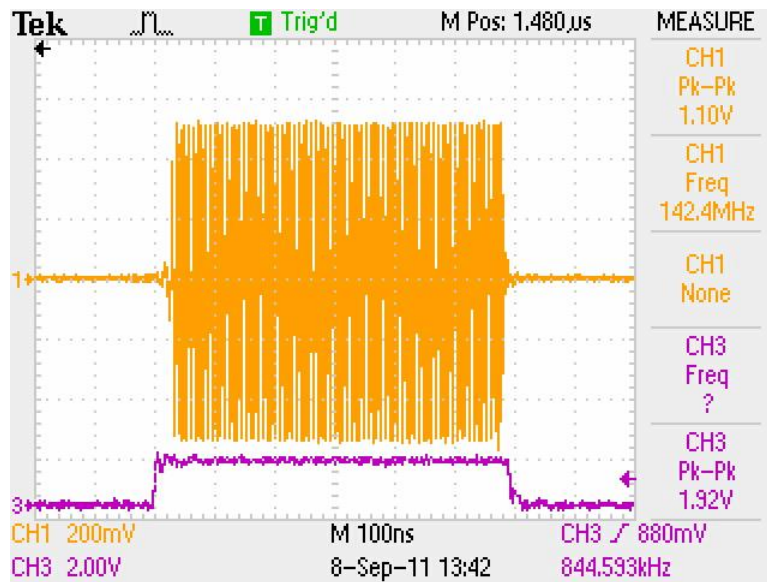


**Figure 7:** A 600 ns RF pulse at 10 MHz is shown in the base band with no digital up-conversion features turned on.

# PulseBlasterDDS-IV-1000

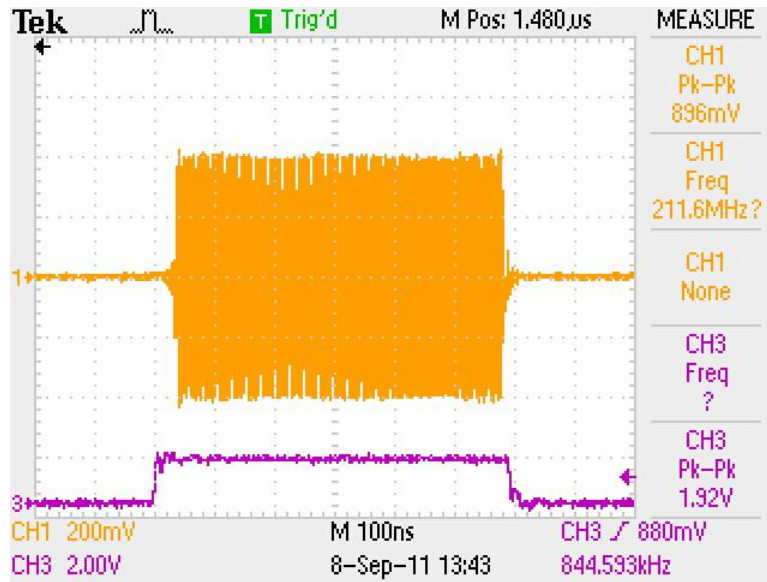


**Figure 8:** The digital up-conversion option “Shifted DC with Pre-modulation” has been applied to the signal from Figure 7. The signal is shifted up 62.5 MHz.

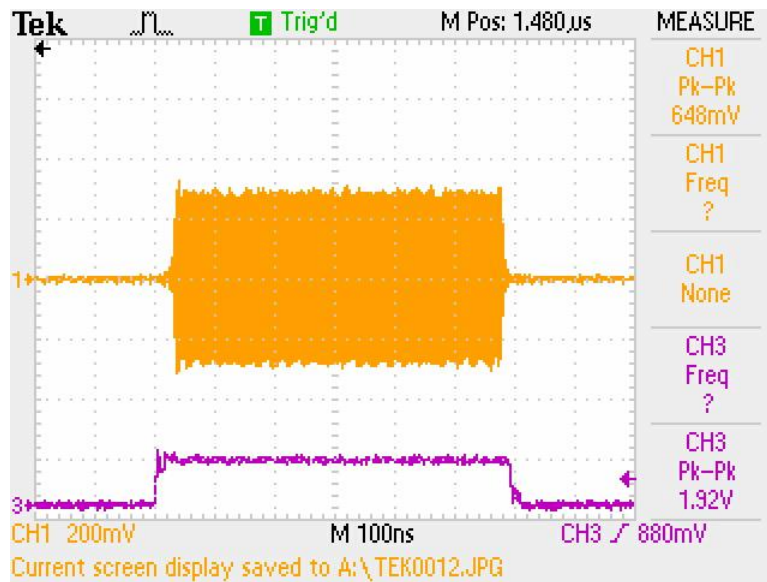


**Figure 9:** The digital up-conversion option “Fs/8” has been applied to the signal from Figure 7. The signal is shifted up 125 MHz.

# PulseBlasterDDS-IV-1000

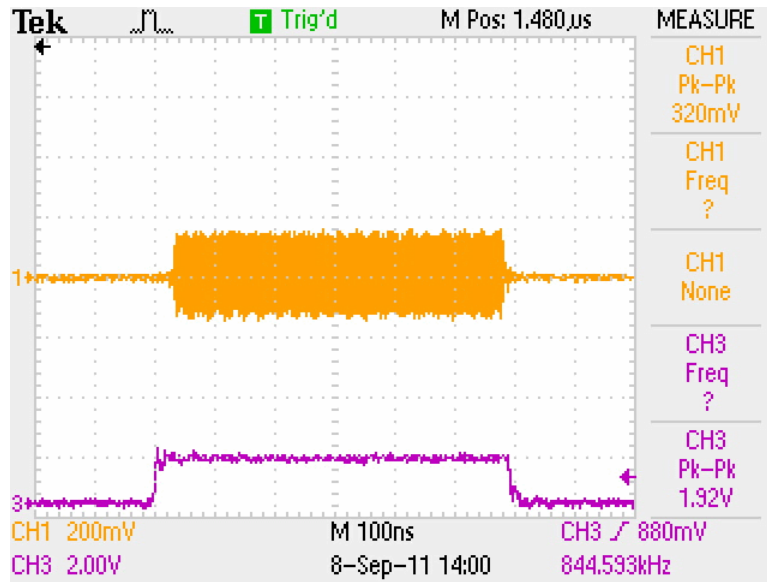


**Figure 10:** The digital up-conversion option “Shifted Fs/8 with Pre-modulation” has been applied to the signal from Figure 7. The signal is shifted up 187.5 MHz.

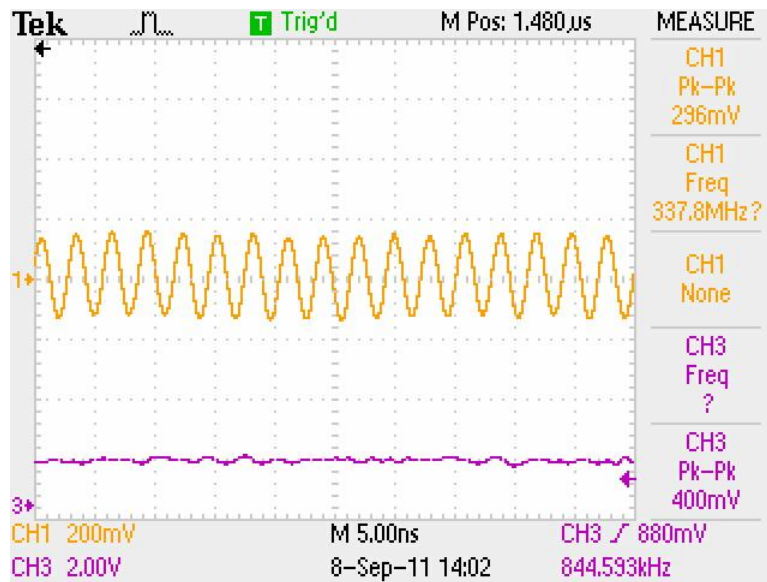


**Figure 11:** The digital up-conversion feature “Fs/4” has been applied to the signal from Figure 7. The signal has been shifted up 250 MHz.

# PulseBlasterDDS-IV-1000



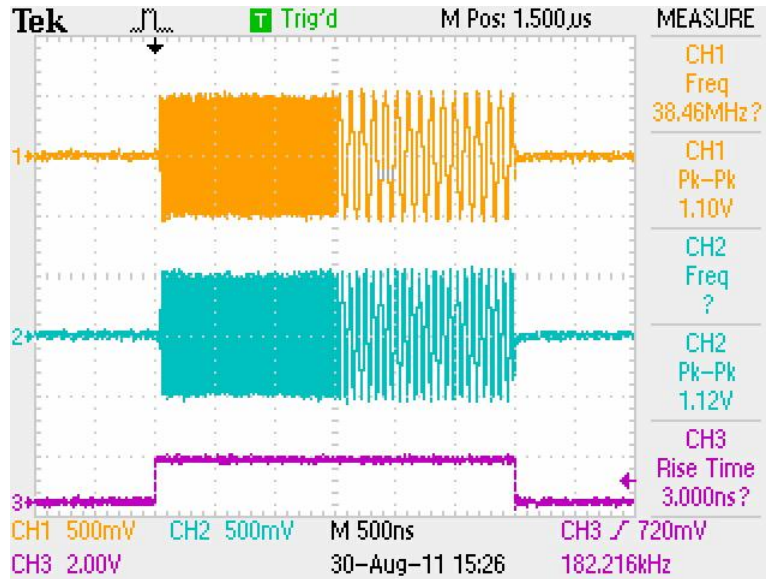
**Figure 12:** The digital up-conversion feature “Shifted Fs/4 with Pre-modulation” has been applied to the signal from Figure 7. The signal has been shifted up 312.5 MHz.



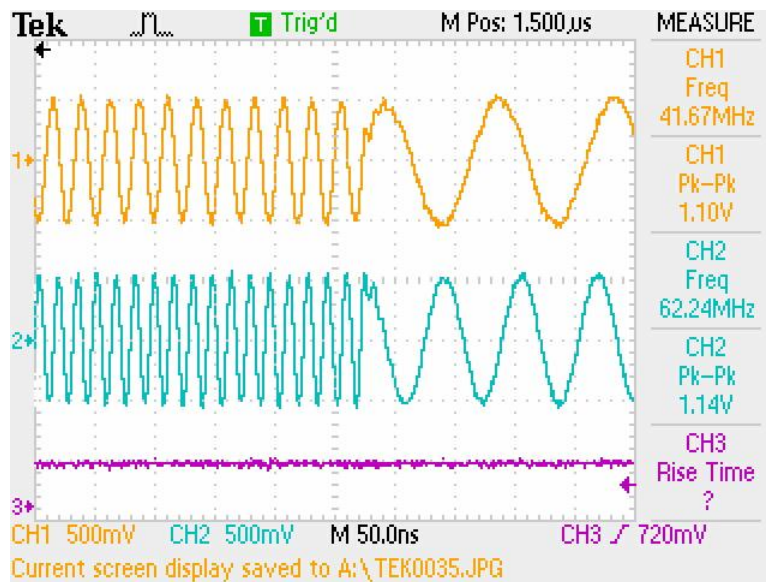
**Figure 13:** We have zoomed in on the signal in Figure 12 in order to show the integrity of the sinusoid. The signal is attenuated due to the oscilloscope.

# PulseBlasterDDS-IV-1000

Figure 14 below shows the agile frequency switching capability of the PulseBlasterDDS-IV.

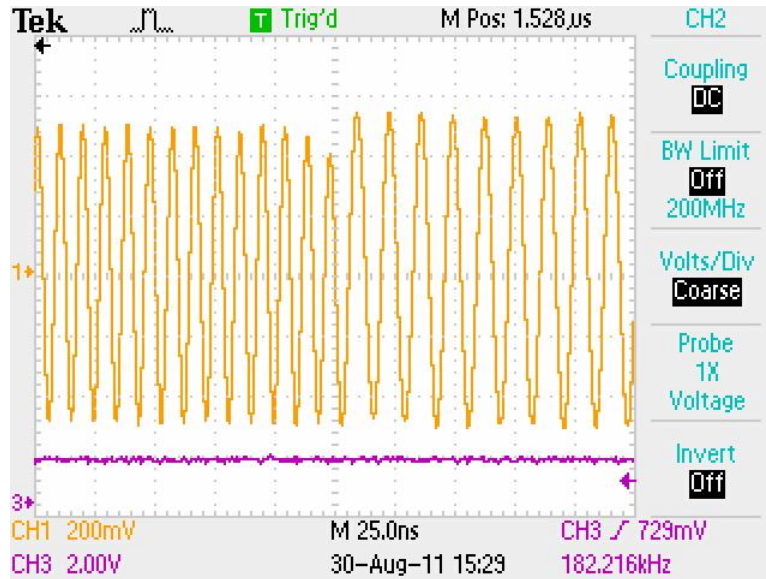


**Figure 14:** A demonstration of the agile frequency switching capabilities of the DDS-IV system. Channel 1 shows a transition from 40 MHz to 10 MHz and channel 2 shows a transition from 60 MHz to 15 MHz. The TTL pulse has been compensated to synchronize the TTL pulse with the RF pulse.

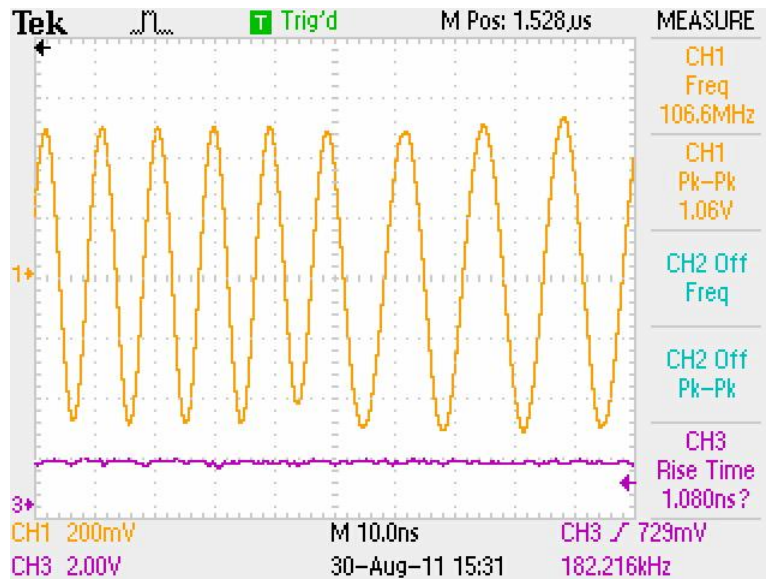


**Figure 15:** This screen capture shows the same signals from Figure 14 but we have zoomed in on the frequency transitions. You can see that the frequency switching is instantaneous.

# PulseBlasterDDS-IV-1000

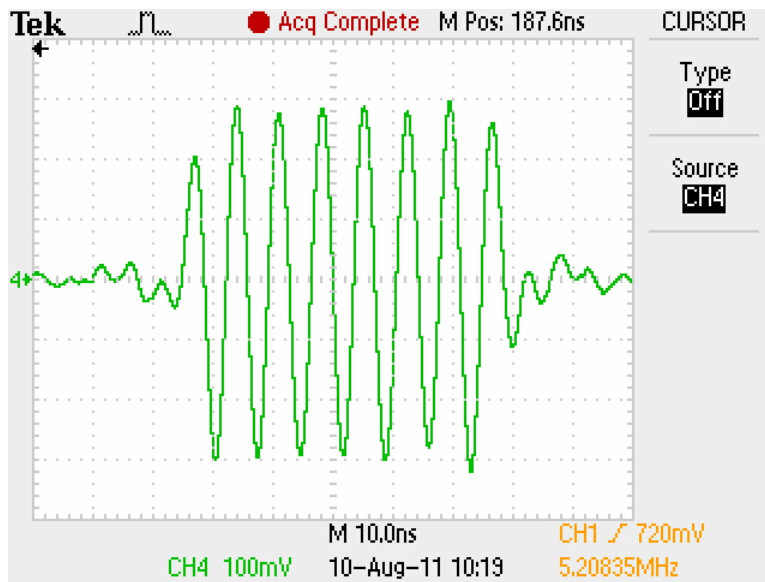


**Figure 16:** In this example we take a closer look at the signal on channel 1 from Figure 14. The AD9148 digital up-conversion features have been enabled to increase the frequency of the RF output. With AD9148 shifted DC coarse modulation and pre-modulation enabled the resulting signal transitions from 102.5 MHz to 72.5 MHz.



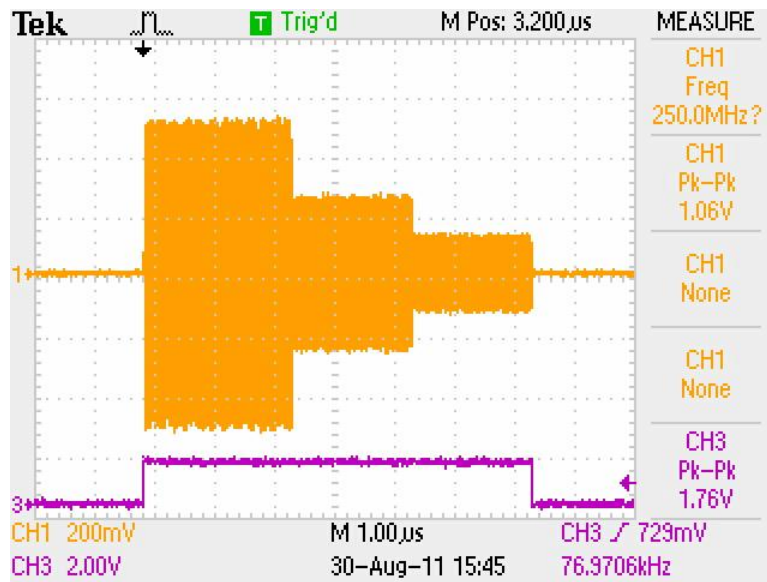
**Figure 17:** This image shows the same signal from Figure 16 but we have zoomed in on the frequency transition. The transition is still instantaneous with AD9148 digital up-conversion enabled.

# PulseBlasterDDS-IV-1000

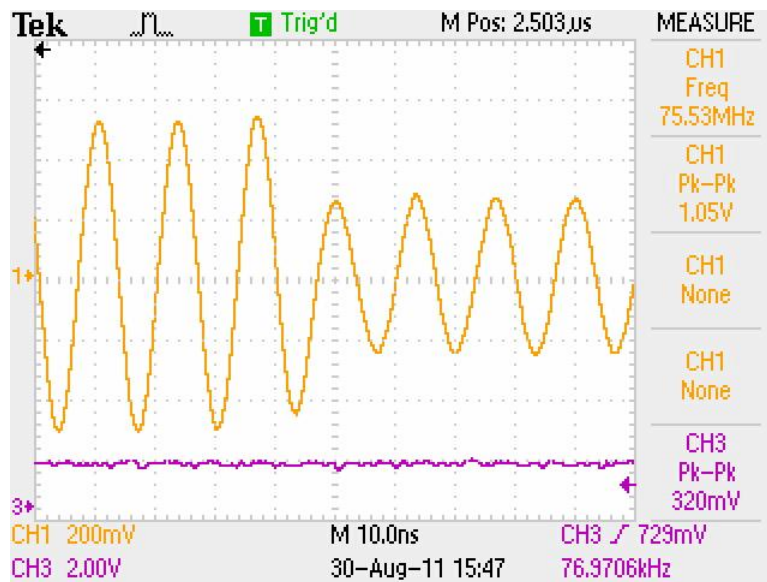


**Figure 18:** The above images shows a 60 ns RF pulse at 135 MHz.

# PulseBlasterDDS-IV-1000



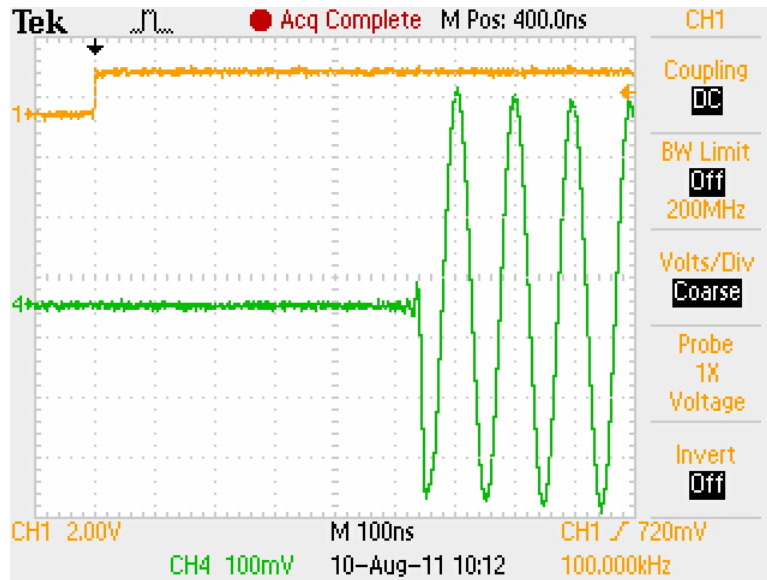
**Figure 19:** This image demonstrates the agile amplitude switching of the DDS-IV. A 75 MHz wave is shown switching from full scale to half scale and finally to quarter scale voltage output.



**Figure 20:** This image shows the same signal as in Figure 19 but we have zoomed in on the transition from full scale to half scale voltage.

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The next image demonstrates the effects of the 0.5 us latency, as mentioned in Table 1. The frequency of the wave is in the base band at 10 MHz so that it can be seen easily. CH1 shows the TTL pulse while CH4 shows the RF pulse.



**Figure 21:** Demonstration of the 0.5 us latency. There is a 508 cycle delay associated with the AD9148. At 1 GHz this equates to roughly 0.5 us.

The next figure shows how latency compensation can be used to synchronize the TTL pulse with the RF pulse. Once again, the RF wave is in the base band so that it can be seen easily.

# PulseBlasterDDS-IV-1000

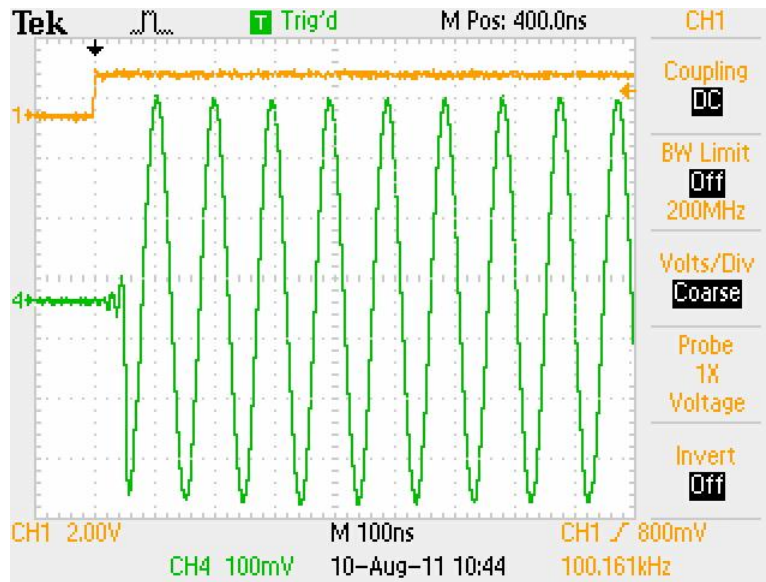


Figure 22: Latency compensation demonstration.

In the figure below, you can see the effects of the latency compensation using a 135 MHz output frequency. This was obtained using the same base band frequency as in Figure 22 above. In this case, the AD9148 digital up-conversion has shifted the frequency by 125 MHz ( $F_s/8$  coarse modulation).

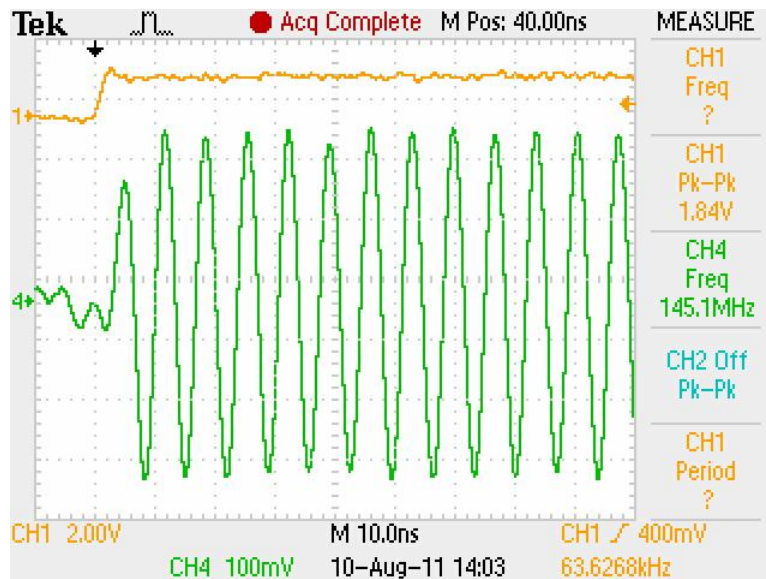


Figure 23: Latency compensation at 135 MHz.

## Instructions

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### *Programming Instructions on to the DDS-IV*

Instructions are programmed to the board using the `pbddsiv_inst()` function. The parameters of this function are show in Table 2. For all the arrays (indicated by a \* before the parameter name), index 0 corresponds to DDS Unit 0 and index 1 corresponds to DDS unit 1.

<pre>int pbddsiv_inst(int addr, int flags, int *oe, int *phase_reset, int *freq, int *phase, int *amp, int inst, int inst_data, double time_sec)</pre>	The <code>pbddsiv_inst()</code> function and it's parameters. This instruction returns a -1 on failure.
<code>int addr</code>	The address to which the instruction will be programmed.
<code>int flags</code>	The 16 bit digital pulse to be output.
<code>int *oe</code>	Output enable for the DDS cores. This field is active-high.
<code>int *phase_reset</code>	Phase reset for the DDS cores. This field is active-high.
<code>int *freq</code>	The chosen frequency register.
<code>int *phase</code>	The selected phase register.
<code>int *amp</code>	The active amplitude register.
<code>int inst</code>	The instruction code. Please see Table 3 for more details.
<code>int inst_data</code>	The instruction data. Please see Table 3 for more details.
<code>double time_sec</code>	The duration of the instruction in seconds.

**Table 2:** Breakdown of the `pbddsiv_inst()` function. The phase register feature is currently unsupported. If you require this feature, please contact SpinCore Technologies.

## Instruction Set

In Table 3 below you can see the instruction set for the PulseBlasterDDS-IV-1000.

Op Code #	Instruction	inst_data field	Function
0	CONTINUE	Unused	Program execution continues to the next instruction.
1	STOP	Unused	Stop execution of program. Aborts the operation of the micro-controller with no control of output states (all TTL values remain from previous instruction). Recommended that prior to the STOP op-code a short interval (minimum six clock cycles) be added to set the output states as desired.
2	LOOP	Number of desired loops (must be at least 1).	Specify beginning of a loop. Execution continues to next instruction. Data used to specify number of loops.
3	END_LOOP	Address of the beginning of the loop.	Specify end of a loop. Execution returns to begging of loop and decrements loop counter.
4	JSR	Address of the first subroutine instruction.	Program execution jumps to beginning of a subroutine.
5	RTS	Unused	Program execution returns to the instruction after JSR was called.
6	BRANCH	Address of the instruction to branch to.	Program execution continues at specified instruction. This behaves like the GOTO statement found in many programming languages.
7	LONG_DELAY	Number of desired loops. Must be at least 2.	Used to long intervals. Data field specifies a multiplier of the delay field. Execution continues at the next instruction.
8	WAIT	Unused	Program execution pauses and waits for a software of hardware trigger to resume it.

**Table 3:** PulseBlaster Instruction Set

## Basic Control Functions

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### **Functions to communicate with the DDS-IV**

These functions are used to establish communication with the PulseBlasterDDS-IV-1000 or to receive information about it or its status. Table 4 contains a description of each one.

<code>int pbddsiv_init()</code>	Used to open communication with the board. This must be called before any other API functions.
<code>int pbddsiv_get_firmware_id()</code>	Returns the firmware ID of the board.
<code>int pbddsiv_set_core_clock(double clock)</code>	Sets the core clock frequency. The input to this function must be 125000000 for proper pulse timing.
<code>int pbddsiv_get_status()</code>	Returns the status of the board.

**Table 4:** Basic Communication Functions.

### **Flow control functions**

The flow control functions allow the board to be triggered or reset. These functions behave identically to the hardware trigger and reset inputs. They are shown below in Table 5.

<code>int pbddsiv_trigger()</code>	Starts program execution.
<code>int pbddsiv_reset()</code>	Resets the program counter 0 and halts program execution.

**Table 5:** Flow Control Functions.

## DDS Core Programming Functions

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These functions are responsible for programming the registers specific to each DDS core. Each function returns a -1 on failure. Table 6 below shows each function and a description of its parameters.

<code>int pbddsiv_select_dds(int dds_num)</code>	Selection which DDS core (0 or 1) to program.
<code>int pbddsiv_set_freq(double freq, int addr)</code>	Set the base-band freq of a particular freq register.
<code>int pbddsiv_set_amp(float amp, int addr)</code>	Sets the amplitude of a chosen register. 1.0 is full scale.
<code>int pbddsiv_set_phase(double phase, int addr)</code>	Programs the phase in a phase register.

**Table 6:** DDS Core Control Functions. The phase register feature is currently unsupported. If you require this feature, please contact SpinCore Technologies.

## Interrupt Control Functions

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The interrupts can be configured and activated through software in addition to being able to be activated through hardware. Table 7 shows the functions associated with the interrupt feature.

<code>int pbddsiv_int_addr_write(int interrupt, int pb_address)</code>	Sets the address associated with a chosen interrupt.
<code>int pbddsiv_set_int_source(int select)</code>	An input of 0 means hardware selection of interrupts and an input of 1 means software selection.
<code>int pbddsiv_set_sw_int(int interrupt)</code>	Selects a particular software interrupt to jump to. Functions just like the hardware interrupt lines.
<code>int pbddsiv_get_current_int()</code>	Returns the currently active interrupt.

**Table 7:** Interrupt Control Functions.

### III. Connecting to the PulseBlasterDDS-IV-1000

#### Front Panel Connector Locations

The PulseBlasterDDS-IV-1000 system is housed in a 3U rack mount enclosure. The front panel contains all of the ports needed to interact with the DDS-IV-1000. There are four main elements on the front panel of the enclosure: the BNC connectors, a female DE9 (sometimes called a DB9) connector, a USB Type-B port and a DC power supply on/off switch. The back panel contains the AC power cord connection and an AC on/off switch.

The BNC connectors provide the means of interfacing with the input and output signals of the PulseBlasterDDS-IV-1000. The RF and digital outputs, 10 MHz reference input clock, and the trigger input are all accessed via BNC connectors. The DE9 connector is used to interface with the interrupt input. The USB port is used to communicate with the host PC. The front panel switch is used to turn the DDS-IV-1000 on and off when the back panel AC switch is also on.

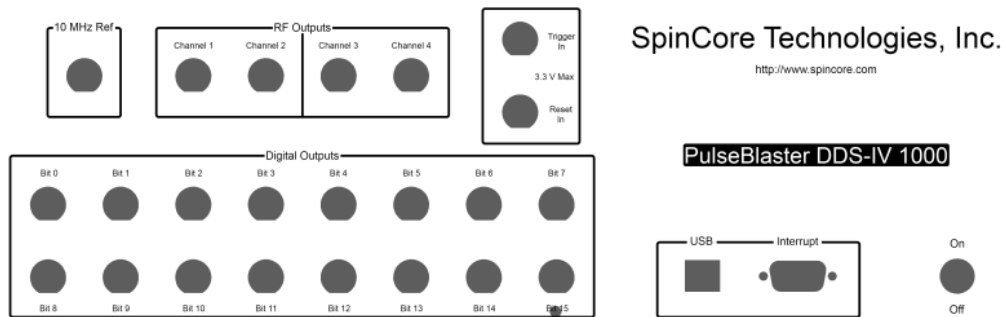


Figure 24: Front panel connector locations.

#### RF Outputs

The PulseBlasterDDS-IV-1000 has four RF outputs, all of which are accessed through female BNC connectors. Figure 25 presents the numbering scheme for these outputs. Please note that independent waveforms are generated by outputs 1 and 3; output 2 is the same as output 1 with a 90 degree phase offset. Similarly, output 4 is a 90 degree phase shifted version of output 3. The source impedance is 50 Ohm.

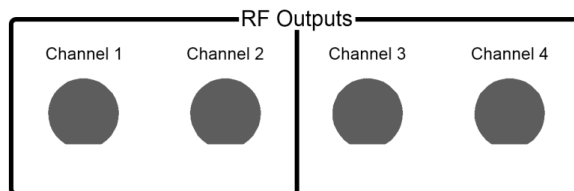


Figure 25: RF BNC output jacks.

## Digital Outputs

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The 16 digital outputs of the PulseBlasterDDS-IV-1000 are accessible through female BNC connectors on the front panel. The numbering of the bits is presented in Figure 26. The required minimum logical high TTL level of 2.5 V is attained when the load impedance is 150  $\Omega$ .

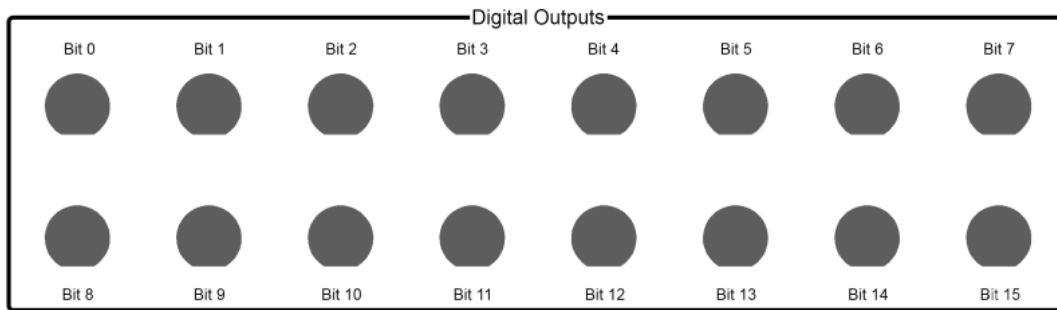


Figure 26: Numerical order of the digital outputs.

## 10 MHz Reference Clock Input

---

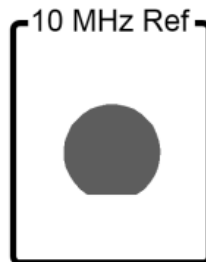


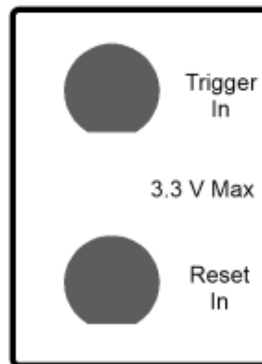
Figure 27: 10 MHz reference clock input label

The PulseBlasterDDS-IV-1000 features a 10 MHz reference clock input that can be used to synchronize the system to an external 10 MHz, square, 50% duty cycle, 3.3V-level clock signal. This signal is sent through a PLL (phase locked loop), which creates the higher clock frequencies required by the PulseBlaster core, DDS cores, and the AD9148 DAC.

The external 10 MHz reference can be connected before the board is powered on or during operation. The PulseBlasterDDS-IV-1000 will automatically begin using the external reference once it detects that it is present. Please note, however, that a power reset is required to switch back to the internal oscillator after removing the external clock source.

## Trigger and Reset Input

---



**Figure 28:** HW trigger and reset input labels

The trigger input is used to start a pulse program that has been loaded into the instruction memory of the PulseBlasterDDS-IV-1000. This input is used in tandem with the DE9 interrupt port, which can be used to configure the instruction memory address that will be read from first when the trigger input is activated.

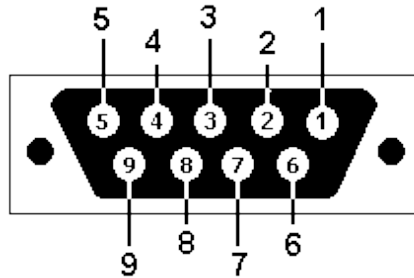
Doing so produces the same results as the `pbddsv_trigger()` API function described in the Basic Control Functions section. The input is normally pulled high and the maximum voltage that can be input to the connection is 3.3V.

The trigger input is active-low, meaning that inputting a low voltage level will cause the PBDDS-IV to be triggered. The board is not triggered on a rising or falling edge. Please note that as long as the input to the trigger is a logical-low voltage level, the board will be triggering.

The reset input is used to reset a pulse program to the beginning (the program counter is reset to 0). The reset input is active-low, meaning that inputting a low voltage level will reset the pulse program running on the PBDDS-IV. This is the same behavior as the `pbddsv_reset()` API function described in the Basic Control Functions section. The input is normally pulled high and the maximum voltage that can be input to the connection is 3.3V.

## Interrupt Input

The DE9 interrupt connector, shown below in Figure 29, is used to control the 256 available interrupts on the PulseBlasterDDS-IV-1000. Please note that in order to use this hardware interrupt control, you must enable hardware interrupts as described in the Interrupt Control Functions section.



**Figure 29:** Pin out of the DE9 Interrupt connector

The pin out for this connector is shown below in Table 8. Be sure to match this pin out exactly if you are creating your own DE9 interrupt cable. Please note that every signal pin is active-high. The maximum voltage level that can be asserted on a signal pin is 3.3 V, and the minimum voltage level is 0 V. As an example, asserting a high logic level on interrupt bits 0, 3, and 4 while hardware interrupts are enabled in the API has the same effect as the `pbddsiv_set_sw_int(0x19)` function call does when software interrupts are enabled. Please note that all the signal pins are weakly pulled high, so if no input is connected then the highest interrupt (0x255) is always asserted in hardware.

Pin Number	Pin Function
1	Interrupt bit 0
2	Interrupt bit 1
3	Interrupt bit 2
4	Interrupt bit 3
5	Interrupt bit 4
6	Interrupt bit 5
7	Interrupt bit 6
8	Interrupt bit 7
9	GND

**Table 8:** Interrupt Input Pin-out

## PulseBlasterDDS-IV-1000

If using a high input impedance oscilloscope to monitor the PulseBlasterDDS-IV-1000, place a resistor that matches the characteristic impedance of the transmission line in parallel with the coaxial transmission line at the oscilloscope input. (e.g., a 50  $\Omega$  resistor with a 50  $\Omega$  transmission line, see Figures 30 and 31 below). When using an oscilloscope with an adjustable bandwidth, set the bandwidth to as large as possible. Failure to do so may yield inaccurate readouts on the oscilloscope.



**Figure 30:** Left - BNC T-Adapter and Right - BNC 50 Ohm resistor





**Figure 31:** BNC T-Adapter on the oscilloscope with coaxial transmission line connected on the left and BNC 50 Ohm resistor connected on the right, to terminate the line.

## IV. Using the AD9148 DAC Config. Software

### Initial Configuration

---

Before correct RF outputs can be generated, the AD9148 DAC software must be configured. Please take the following steps to properly configure the software. Please note that the DAC does not maintain its configuration when powered down.

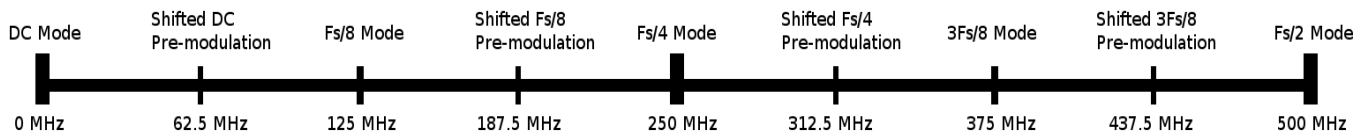
1. Open the AD9148 DAC Software from the Analog Devices/AD9148-EBZ folder in the Start Menu.
2. Go to the AD9516 tab.
  - a) Click on "Use PLL?" to turn it on. Blue color means the PLL is on.
  - b) Set the "Counter B" field to 4.
  - c) Set the "R Div Ratio" field to 2.
  - d) Enter '125' in the field "AD9516 Ref Clk (MHz)"
  - e) Click on "Use Ref Clk" to turn it on.
  - f) Set "Ref Clk Div Ratio" and "DCO Clk Div Ratio" to Divide-by-8
  - g) Uncheck the "Sync With Interpolation" option under "DCO Clk Div Ratio"
  - h) Run the interface module twice to ensure that the PLL is locked (it will light up green) and that the "Output Clock (MHz)" read back shows 1000 MHz.
  - i) Now turn "AD9516 Control" OFF so that these settings are not changed until powering down the system.
3. Go to the Data tab.
  - a) Change "Interpolation" to "8x"
  - b) Click on "Bus Swap" to turn it on.
  - c) Click on "Binary Enable" to turn it on.
  - d) Click on "Q First Enable" to turn it on.
4. Go to the Main DAC tab.
  - a) Set "DAC Gain" fields under the Analog Full-Scale Current Control heading to 1023.
  - b) After doing this, all the "Current" fields should read 30.000mA.
5. Turn on the AD9148 DAC:
  - a) Click on the "Run Continuously" button to turn it on.
  - b) Click the  button in the top left corner of the window.
  - c) After the previous two steps are done, the graphic in the top left corner should look like .
6. The DAC is now ready to output data continuously from the PulseBlasterDDS-IV-1000 cores.

## Configuring the Output Frequencies

---

Once the AD9148 DAC software is configured according to the previous section, you may generate correct output waves using the PulseBlasterDDS-IV-1000. The following are the considerations involved in producing your desired frequencies.

- The PulseBlasterDDS-IV-1000 API allows you to input base-band frequencies of up to 62.5 MHz. Please see the DDS Core Programming Functions section for more details.
- On the Data tab of the AD9148 DAC software, you can configure center frequencies to cover the range from DC to 400 MHz. See Figure 32 below:



**Figure 32:** Frequency bands corresponding to their respective coarse modulation modes.

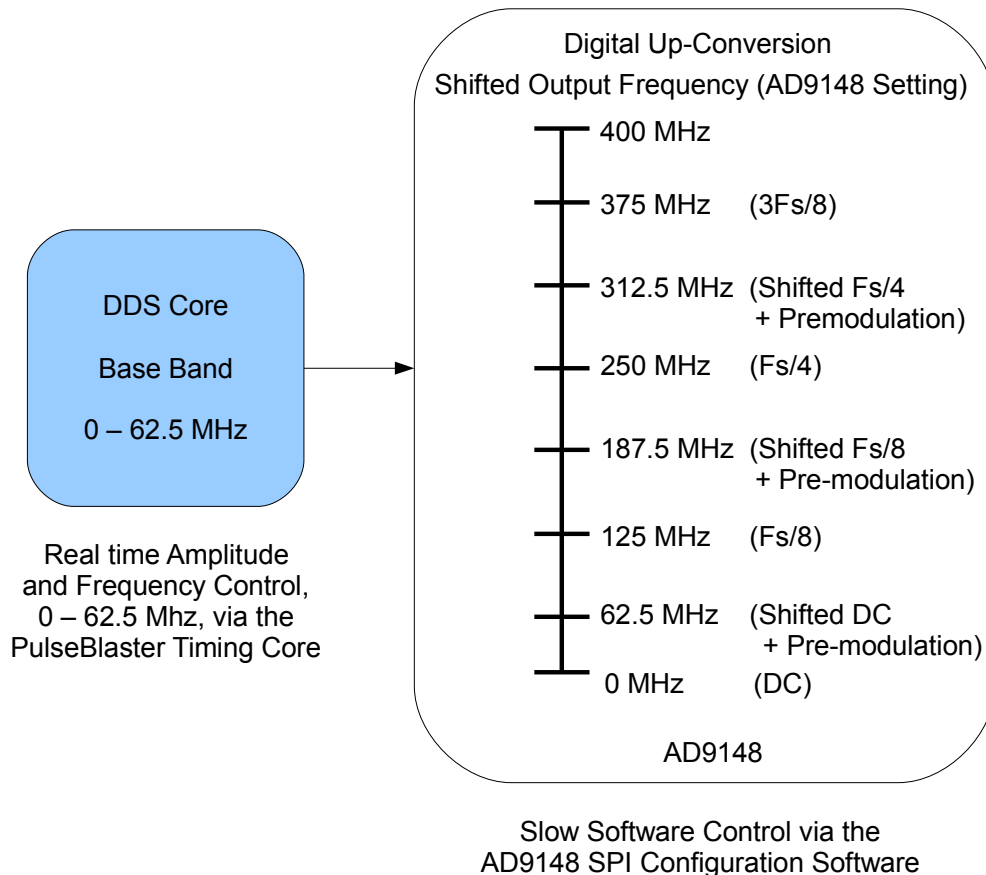
- The output frequency will be the sum of the input base-band frequency and the center frequency selected in the DAC software.
- To “Course Modulation” and “Pre-modulation” settings in the DAC software allow you to choose from the following center frequencies:
  - DC mode: 0 MHz (baseband signals)
  - Shifted DC mode with pre-modulation: 62.5 MHz
  - Fs/8 mode: 125 MHz
  - Shifted Fs/8 mode with pre-modulation: 187.5 MHz
  - Fs/4 mode: 250 MHz
  - Shifted Fs/4 mode with pre-modulation: 312.5 MHz
  - 3\*Fs/8 mode: 375 MHz
  - Shifted 3\*Fs/8 mode with pre-modulation: 437.5 MHz

# PulseBlasterDDS-IV-1000

- Here are some examples of the basic operation:
  - Base-band frequency of 30 MHz with DC mode: 30 MHz output frequency
  - Base-band frequency of 30 MHz with  $F_s/8$  mode: 155 MHz output frequency
  - Base-band frequency of 30 MHz with shifted  $F_s/8$  mode and pre-modulation: 217.5 MHz output frequency
  - Base-band frequency of 45 MHz with shifted  $F_s/4$  mode and pre-modulation: 357.5 MHz output frequency
- ***Do not use the non-shifted modes with Pre-modulation or the shifted modes without Pre-modulation.*** This may cause unpredictable results:
  - Base-band frequency of 2 MHz with shifted  $F_s/8$  mode: unpredictable operation
  - Base-band frequency of 2 MHz with  $F_s/8$  mode: 127 MHz output frequency
  - Base-band frequency of 2 MHz with  $F_s/8$  mode and Pre-modulation: unpredictable operation
  - Base-band frequency of 2 MHz with shifted  $F_s/8$  mode and Pre-modulation: 189.5 MHz output frequency

## Real Time vs. Slow Software Control

As stated above, the PulseBlasterDDS-IV-1000 API allows you to input base-band frequencies of up to 62.5 MHz in real time using the DDS cores and PulseBlaster timing core. Using the AD9148 DAC software, you can shift the DDS frequencies up to cover the range from DC to 400 MHz. See the figure below for more information.

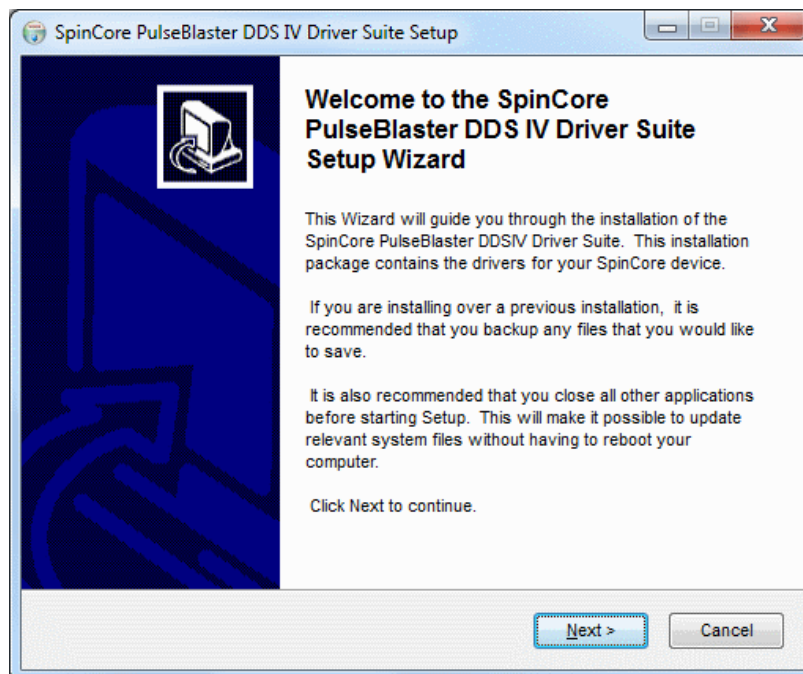


**Figure 33:** The slow software AD9148 interface is used to output frequencies across the entire output range, DC to 400 MHz. The PulseBlaster timing core provides real time amplitude and frequency control in the base band (0 to 62.5 MHz)

## V. Installing the PBDDS-IV-1000

### Installing the SpinCore PulseBlasterDDS-IV-1000 Software

- The installer will guide you through the installation of the Application Program Interface (API), its dependencies, and example programs.
- The first section will welcome you to the installation.



**Figure 34:** This is the first window you will see when running the installer.

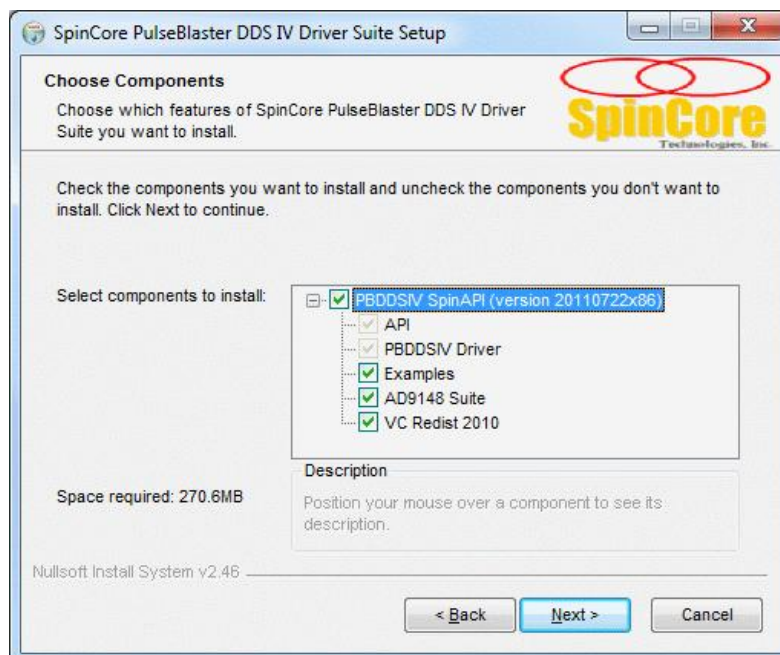
# PulseBlasterDDS-IV-1000

- The second stage is our license. Please read it, and then click “I Agree” to continue.



**Figure 35:** The license agreement for the DDS-IV-1000 driver and software suite.

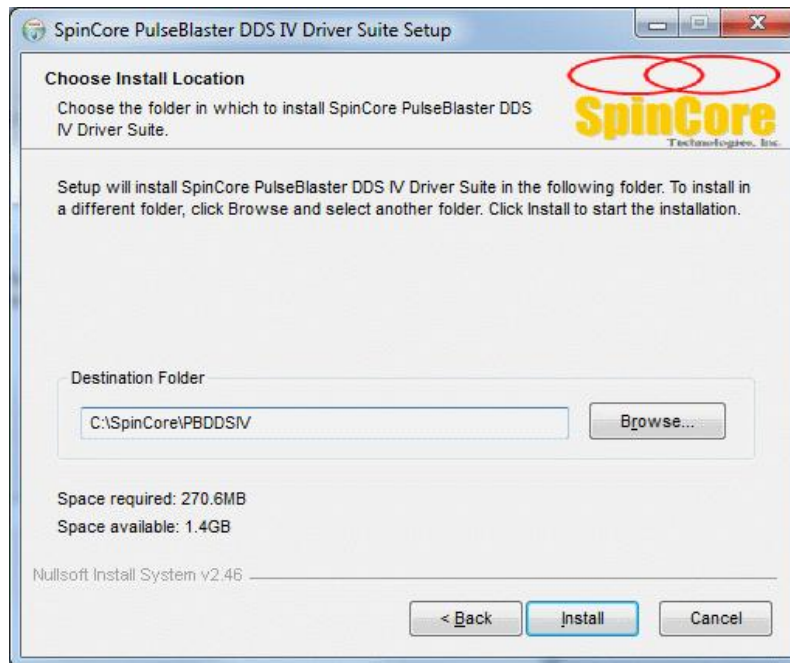
- The third screen allows you to select which components you wish to install. If this is your first installation, please select all of them. Click 'Next.'



**Figure 36:** Select the features you want installed then click next.

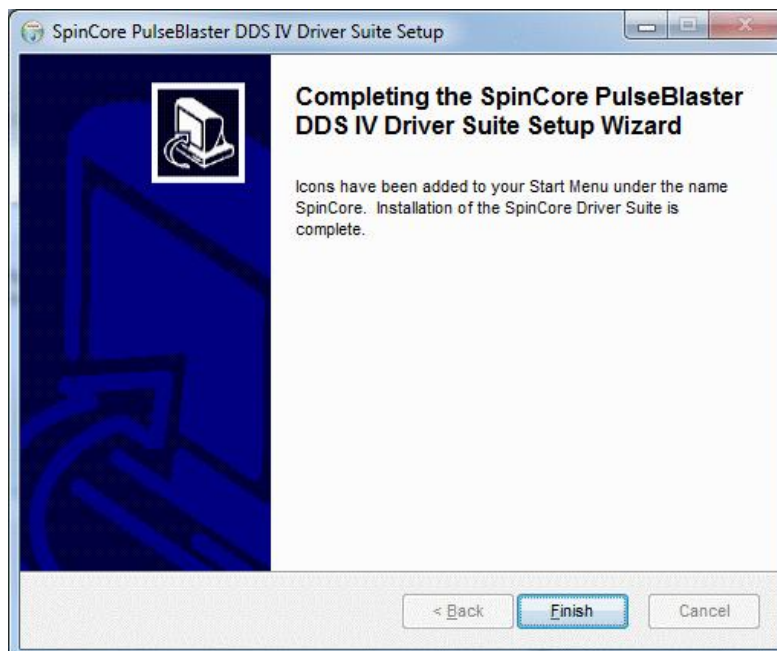
# PulseBlasterDDS-IV-1000

- The fourth screen lets you choose the installation location. The default location should be fine.



**Figure 37:** Choose the installation destination (default recommended).

- Setup will then proceed to install your selected components. If you have selected them, the AD9148 Suite and VC Redist 2010 will have installers that pop up during this process. Instructions for these installations are in the next section of this document.
- Once all of the components have installed, click 'Finish' to close the installer.



**Figure 38:** Congratulations! The installation is a success.

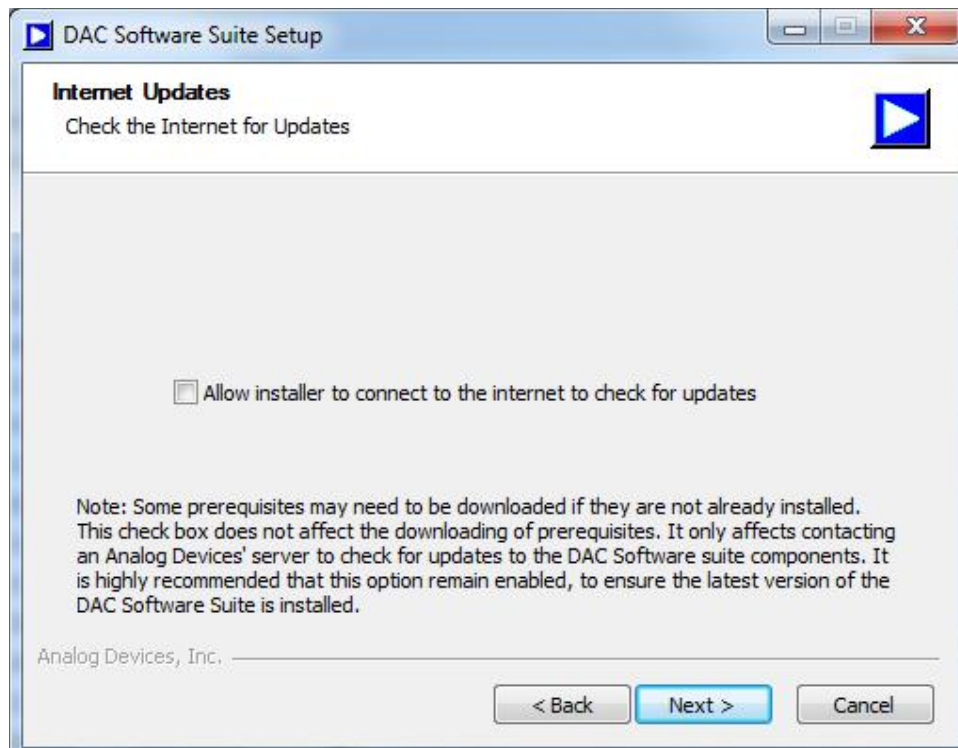
## Installing the Analog Devices 9148 DAC Configuration Software

### Description:

- The software for the AD9148 is used to configure the DAC controller so that the correct frequency shifts can be achieved. The software communicates with the AD9148 through USB via the on chip Serial Peripheral Interface, or SPI.

### Installation Instructions:

- The software suite is included in the provided installer package. It will run automatically during installation if you select it.
- The first stage of the installation wizard will ask if you want to check for internet updates. NOTE: Please make sure to uncheck the box, as the installer will stall if it is checked. Click next.

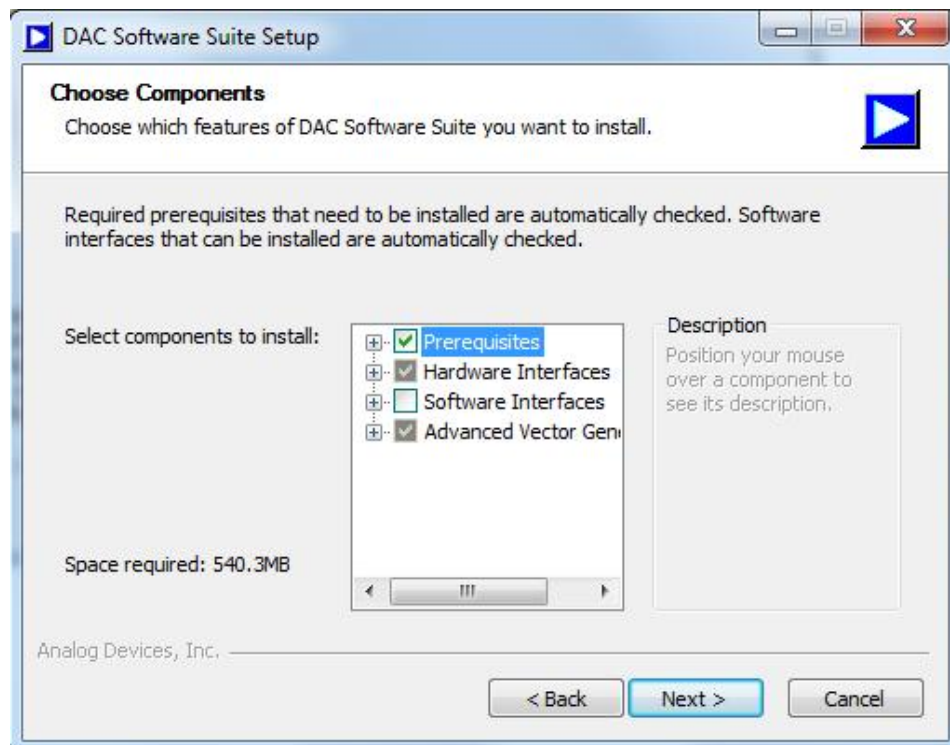


**Figure 39:** Do not allow the installer to connect to the internet to check for updates. The installer will freeze while searching for updates and fail.

# PulseBlasterDDS-IV-1000

- At the “Choose Components” stage, check the "prerequisites box," but leave the others as they are. After clicking next, any of the software requirements that you do not have will be installed before DAC software suite installation continues. For reference, the required prerequisites are:

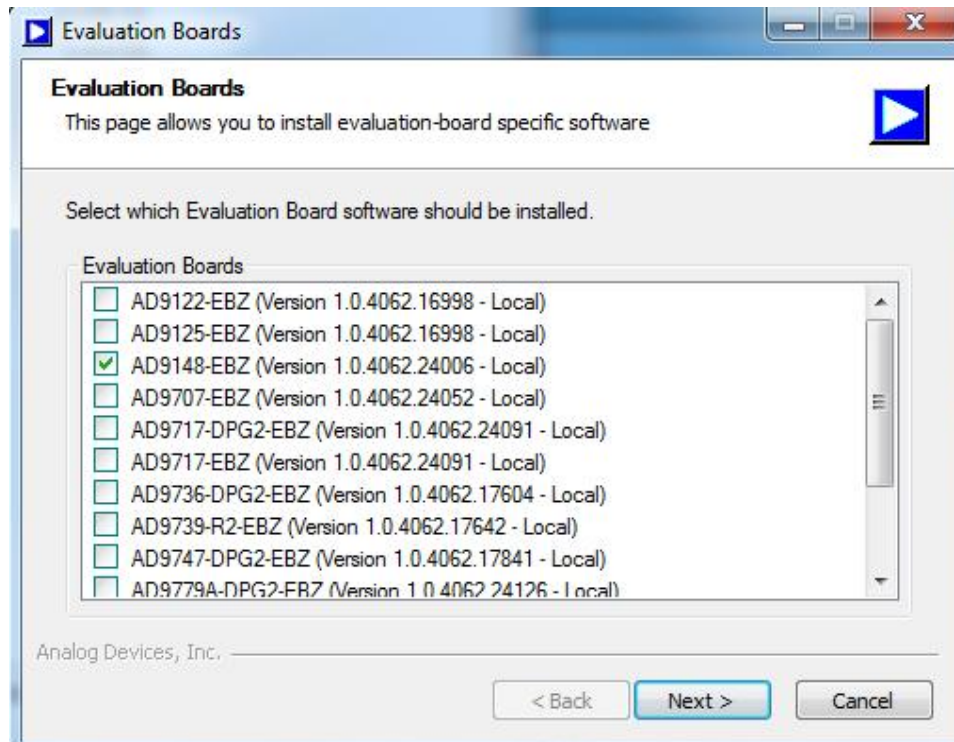
1. Microsoft Windows Installer 3.1 or later
2. Microsoft .NET Framework version 3.5 or later
3. National Instruments VISA Runtime Version 4.5 or later
4. National Instruments LabVIEW Runtime Version 7.1.1 (later versions are not compatible)



**Figure 40:** Be sure to install the prerequisites.

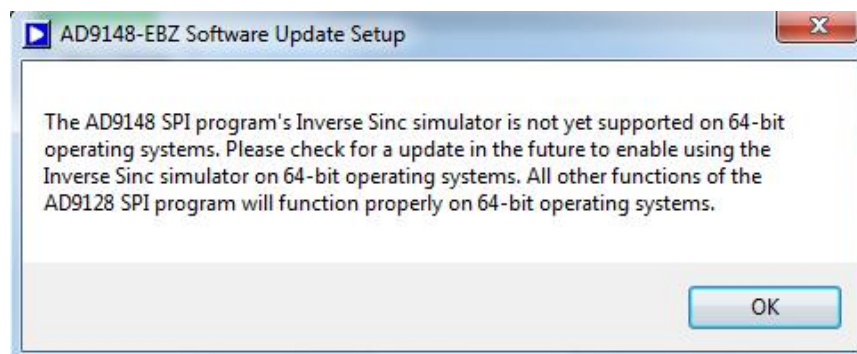
# PulseBlasterDDS-IV-1000

- After all of the prerequisites have been installed, you will come to the “Evaluation Board” prompt. Uncheck all of the boxes except for the 'AD9148-EBZ', then click next.



**Figure 41:** Only the AD9148-EBZ software needs to be installed for the DDS-IV-1000.

- If you receive the following message (if you are using a 64-bit system) after clicking next, press OK, as it will not adversely affect the functionality of the PulseBlasterDDS-IV-1000 system. After this, the installation is complete.



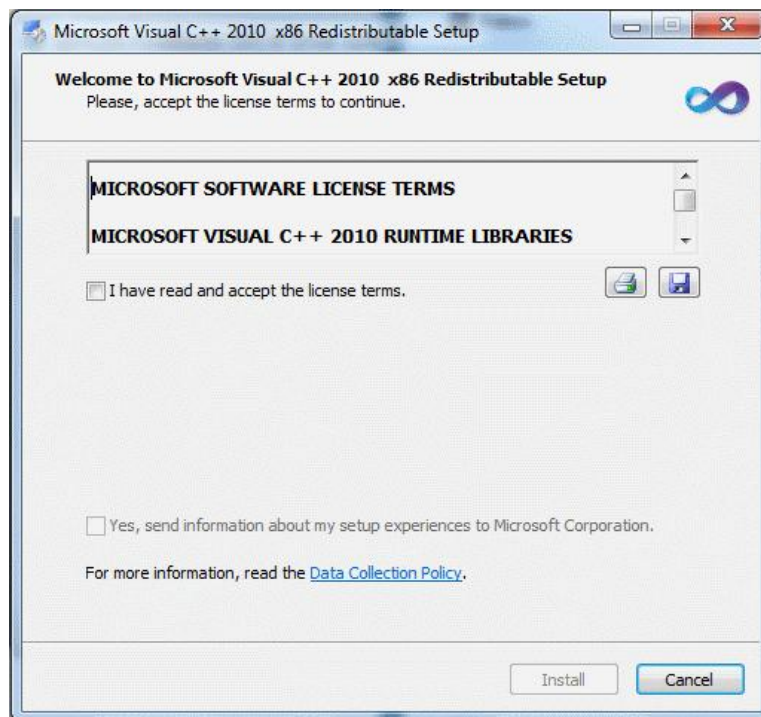
**Figure 42:** This warning will pop up if you are using a 64-bit operating system. It can be ignored. The Inverse Sinc simulator is not used by the DDS-IV-1000.

## Installing the VC Redist 2010 Software

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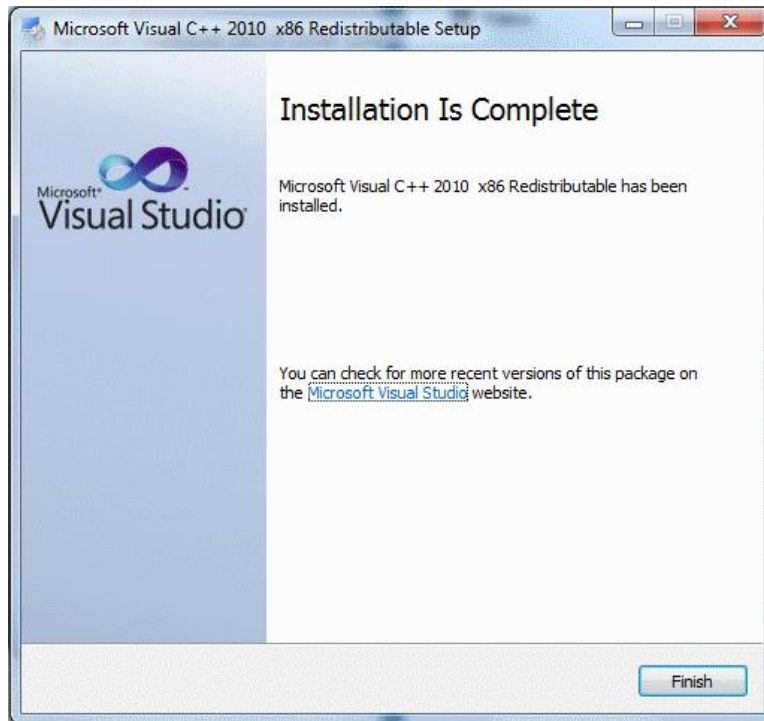
### Installation Instructions:

- The software suite is included in the provided installer package. It will run automatically during installation if you select it.
- You will see the window shown in Figure 43. Select “I have read and accept the license terms.” then click the “Install” button. The remainder of the installation is fully automated. You will see the window shown in Figure 44 when the installation is complete. Click the 'Finish' button to finalize the DDS-IV-1000 software installation.

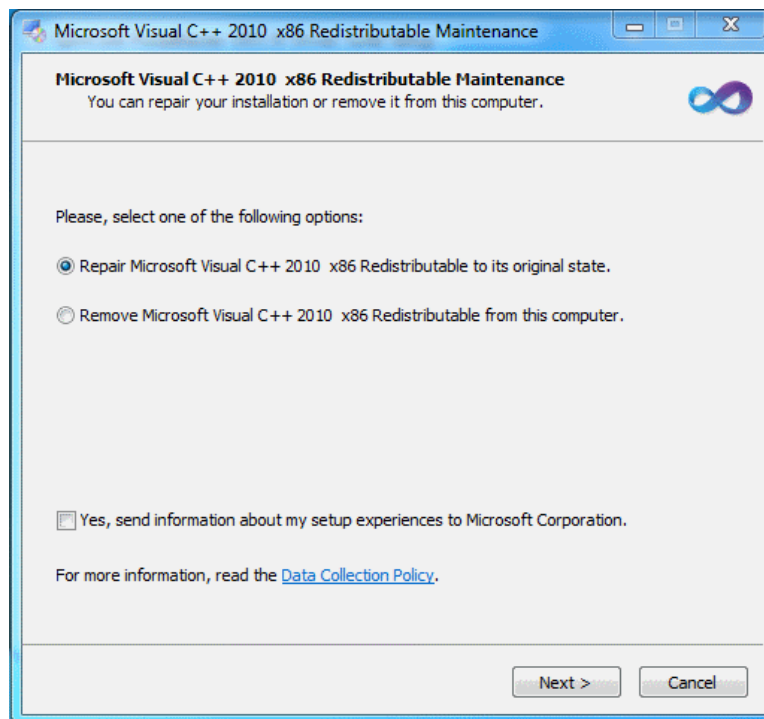


**Figure 43:** Do not remove the Visual C++ redistributable if you already have it installed on your computer.

- If you already have the Visual C++ 2010 Redistributable installed on your computer then you will see the window shown in Figure 45. Do not remove your current installation. Choose the 'Repair' option and the automated installer will continue.



**Figure 44:** The VC Redist 2010 software has been successfully installed.



**Figure 45:** Choose 'Repair' if you already have VC Redist 2010 installed on your computer.

## **Hardware Setup and Verification**

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To set up the PBDDS-IV-1000 hardware:

1. Connect the power cable to the 100 – 240 VAC power supply input on the back panel of the enclosure. Make sure the power supply is powered on.
2. Connect a USB Type B cable to the USB connection on the front panel of the enclosure. Connect the other end to your PC.
3. Use the toggle switch on the front panel to power the system on and off.

After installing the PBDDS-IV-1000 API and setting up the hardware for the first time, we recommend running the provided example programs to verify that your device is functional. The default location of these example programs is “Start > Programs > SpinCore > PulseBlasterDDS-IV Examples.”

## **VI. Contact Information**

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## **VII. Document Information**

A detailed revision history is available by contacting SpinCore Technologies, Inc at the address above.

If you have any feedback or questions, do not hesitate to contact us. We look forward to hearing from each and every one of our customers!

From everyone at SpinCore, we appreciate you reading this manual to learn about your product.